ABSTRACT

A method of defining a conductive gate structure for a MOSFET device wherein the etch rate selectivity of the conductive gate material to an underlying insulator layer is optimized, has been developed. After formation of a nitrided silicon dioxide layer, to be used as for the MOSFET gate insulator layer, a high temperature hydrogen anneal procedure is performed. The high temperature anneal procedure replaces nitrogen components in a top portion of the nitrided silicon dioxide gate insulator layer with hydrogen components. The etch rate of the hydrogen annealed layer in specific dry etch ambients is now decreased when compared to the non-hydrogen annealed nitrided silicon dioxide counterpart. Thus the etch rate selectivity of conductive gate material to underlying gate insulator material is increased when employing the slower etching hydrogen annealed nitrided silicon dioxide layer.